

## ABSTRACT

Impurity ions are implanted into the silicon layer of an SOI substrate to achieve an ion concentration distribution which inhibits for a reduction in threshold voltage (V<sub>th</sub>-rolloff) as a gate length is reduced. A reduction in potential barrier which runs from a drain region side is effectively inhibited to counter short channel effects resulting from a reduction in gate length attendant with miniaturization of SOI-MOSFETs.

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